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09/524,942	03/14/2000	David J. McDonnell	042390.P6357C	8992

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EXAMINER
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ELMORE, REBA I

ART UNIT	PAPER NUMBER
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2187

13

DATE MAILED: 02/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/524,942

Applicant(s)

MCDONNELL ET AL.

Examiner

Reba I. Elmore

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 13-60 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 45-60 is/are allowed.
- 6) ☒ Claim(s) 13-44 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

1. Claims 13-60 are presented for examination.

### *Specification*

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *35 USC 102*

3. The rejection of claims 13-24 and 28-44 as being anticipated by Martin et al. is **withdrawn** from the previous office action

### *35 USC § 103*

4. The rejection of claims 25-27 as being unpatentable over Martin et al. is **withdrawn** from the previous office action.

5. The following new rejection is now given due to the amendment.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 13-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. in view of Keeth et al.

Martin teaches the present invention (claims 13, 23 and 37) an apparatus and method (e.g., see the Background of the Invention section of the reference), the apparatus and method comprising:

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a host side region having a memory access request input and a memory command packet chunk output being taught as a command packet, CDN, from the command bus (e.g., see col. 5, line 65 to col. 6, line 12), a memory command packet chunk being a portion of a memory command packet, the host side region to be clocked by a first clock as being taught as the processor clock frequency of the processor which is equivalent to the host side region of the system (e.g., see col. 1, line 9 to col. 2, line 54);

a memory side region having a memory command packet chunk input coupled to the memory command packet chunk output, the memory side region to be clocked by a second clock with the operating speed of the memory devices being different from the processor operating speed as the memory controller for the system memory devices using a clock frequency substantially lower than the clock frequency of the processor (e.g., see col. 1, line 51 to col. 2, line 5);

the second clock different than the first clock with a first and second clock being taught as a master clock signal and a data clock signal (e.g., see col. 2, lines 55-62);

a memory coupled to the memory side region (e.g., see Figure 3, elements 80a-80h); and,  
a DRAM memory coupled to the memory side region (e.g., see col. 1, line 51 to col. 2, line 39).

Martin teaches the above elements of the present invention, however, this reference does not specifically teach details of the memory being connected to the processor through a memory controller. Keeth teaches the same basic system as Martin and includes the use of a memory controller for accessing the synchronous DRAM at the slower operating clock frequency required by the memory devices. It would have been obvious to one of ordinary skill in the art at

invention was made to combine the teaches of Keeth with the teaching of Martin because the teachings of Keeth are additional improvements to the Martin invention. The Keeth reference describes the additional features for the same basic system of Martin and is therefor combinable with the Martin reference.

As to claim 14, Martin teaches the memory command packet chunk output further comprises a row output and a column output as separate row latches and column latches (e.g., see col. 5, line 55 to col. 6, line 27).

As to claims 15 and 29, Martin teaches the host side memory controller region further comprises a scheduler coupled to the memory access request input with the scheduler being equivalent to a sequencer for sequencing the output of the command latches , the scheduler configured to generate the memory command packet (e.g., see col. 5, line 55 to col. 6, line 27).

As to claims 16 and 30, Martin teaches the scheduler is coupled to a queue as such a system using read and write buffers (e.g., see col.35, line 32 to col. 4, line 21).

As to claims 17, 31 and 39-41, Martin teaches the memory command packet is a row command to activate a memory row by pre-charging the memory row (e.g., see col. 7, lines 18-31).

As to claims 18, 32 and 42-44, Martin teaches the memory command packet is a column command to read or write to/from a DRAM memory device (e.g., see col. 4, lines 23-54 and col. 7, lines 18-31).

As to claims 19 and 33, Martin teaches the scheduler further comprises logic to determine when resource conflicts in that circuitry is present to resolve latching a defective column by latching a redundant column (e.g., see col. 4, line 55 to col. 5, line 35).

As to claims 20 and 34, Martin teaches the host side memory controller region further comprises a second memory command packet chunk output (e.g., see col. 5, line 55 to col. 6, line 27).

As to claims 21 and 35, Martin teaches the second clock is faster than the first clock as the processing speed being much faster than the speed of the memory banks (e.g., see Figure 2).

As to claims 22 and 36, Martin teaches the host side memory controller region is configured to present a second memory command packet chunk upon the second memory command packet chunk output, the second memory command packet chunk a portion of a second memory command packet (e.g., see col. 5, line 55 to col. 6, line 27).

As to claim 24, Martin teaches an external agent configured to read and write to the memory via the memory controller (e.g., see col. 5, line 55 to col. 6, line 27).

As to claim 28, Martin teaches the memory command packet chunk output further comprises a row output and a column output (e.g., see Figure 2).

Martin teaches the independent and intervening claims as given above. Martin does not specifically teach an external agent connected to the memory subsystem having a processor, graphics subsystem and/or an expansion bus master, however, these types of components are common well known elements to be connected to a memory subsystem and official notice is taken thereof. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an external agent having a processor, a graphics subsystem and/or an expansion bus master because these components connected to a memory subsystem provide a wide variety of available usability and lets a user perform even more tasks. An external agent which would be connected to the memory subsystem would normally have a processor and a

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graphics subsystem to provide flexibility which is desirable for a multitude of computer driven activities. An expansion bus provides additional I/O support which is also desirable in computer systems.

8. Newly added claims 45-60 read over the art of record.

***Response to Applicant's Remarks***

9. Applicant's arguments with respect to claims 13-44 have been considered but are moot in view of the new ground(s) of rejection.

10. As to the remarks concerning the 'theory of the rejection', a theory of the rejection was not presented to the applicant. The level of ability for applying art to reject claims is that of 'one of ordinary skill in the art' and as such the rejection is not required to be explained to the level of understanding for a novice or for one of less than ordinary skill in the art.

11. As to Martin not being directed to a memory controller, this is not true. The reference in the background of the invention in columns 1-4 discusses the conventional use of a memory controller for system having memory devices, such as DRAMs, which operate at a slower clock frequency than the processor. Martin describes using a memory controller typically for this purpose and then gives details in the detailed description for using elements other than a memory controller for speeding up the clock frequency needed for the operation of the memory.

***Action is made Final***

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Conclusion***

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (703) 305-9706. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (703) 308-1756. Additionally, the official fax phone number for the art unit is (703) 746-7239. The after-final fax phone number for the art unit is (703) 746-7238. The fax phone number for drafts or non-official communications is (703) 746-7240.



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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center receptionist whose telephone number is (703) 305-3800/4700.



Reba I. Elmore  
Primary Patent Examiner  
Art Unit 2187

February 2, 2004